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(54) High temperature superconductivity in strained Si/SiGe

(57) A structure based on strained Si/SiGe that has high temperature superconductivity is disclosed. The structure for carrying superconducting current includes a substrate (12); a first epitaxial P type semiconductor layer (14), which is under compressive strain, for transporting holes; a second epitaxial barrier layer (20) positioned on the first layer (14); and a third epitaxial N type semiconductor layer (24), which is under tensile strain, for transporting electrons. The barrier layer (30) is thick enough to restrict recombination of electrons and holes, yet the barrier layer (30) is thin enough to permit coulomb force attraction between the electrons and holes to form electron-hole pairs. The first and second layers (14,20) include SiGe, such as $Si_{1-x}Ge_x$, where x is 0.6-0.8 for the first layer (14), and 0.3-0.4 for the second layer (20). The third layer (24) includes Si.

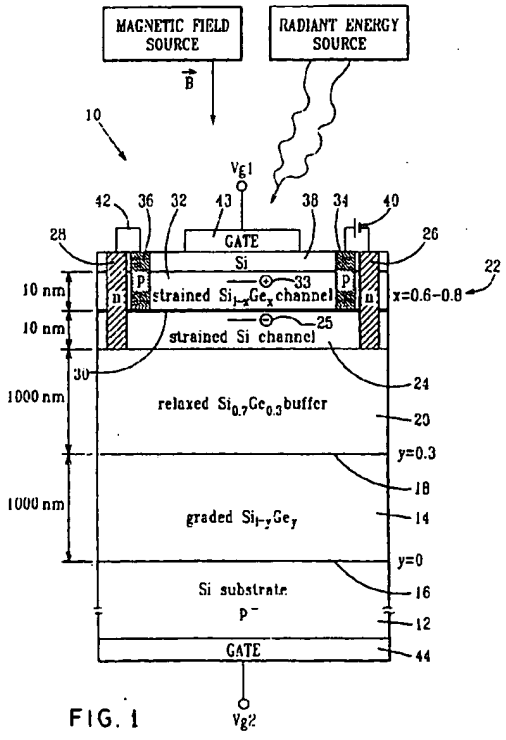


FIG. 1

EP 0 828 296 A2

Description

The present invention is directed to a high temperature superconducting semiconductor structure, and more particularly, to a semiconductor structure having strained Si/SiGe layers separated by a thin SiGe barrier layer.

Superconductors are of great interest for dissipationless transmission and for use in magnetic detectors, among others. Several drawbacks prevent wide use of superconductors, such as the need for excessively low temperatures and incompatibility with standard silicon (Si) technology. Conventional superconductors require low temperature in order to become superconducting, which makes their commercial use quite limited.

Advances in superconductivity have been due to improved electron mobility/conductivity by applying superlattices or strained layers. However, satisfactory superconductors that operate at relatively high temperature, and are compatible with silicon technology have not been achieved. Thus, although high temperature superconductors have been realized, such conventional high temperature superconductors are not fully compatible with standard Si technology, which is the main driver of the semiconductor industry.

Therefore, there is a need for high temperature superconductors that are compatible with conventional Si technology.

The object of the present invention is to provide a superconducting semiconductor structure that eliminates the problems of conventional superconductors.

Another object of the present invention is to provide a structure that is superconducting at relatively high temperatures.

Yet another object of the present invention is to provide a high temperature superconducting structure that is compatible with conventional silicon technology.

A further object of the present invention is to provide a superconducting structure, where the superconductivity is induced by light.

An additional object of the present invention is to provide a gated superconducting structure in which the superconductive state is achieved or destroyed by changing the ratio of electrons to holes by varying gate voltages.

These and other objects of the present invention are achieved by a structure for carrying superconducting current comprising a substrate; a first epitaxial P type semiconductor layer for transporting holes; a second epitaxial barrier layer positioned on the first layer; and a third epitaxial N type semiconductor layer for transporting electrons.

The barrier layer restricts recombination of electrons and holes, while permitting coulomb force attraction between the electrons and holes to form electron-hole pairs. The formation of electron-hole pairs is enhanced due to the small thickness of the barrier layer, which may have a thickness of approximately 5 Å to 30 Å, for example.

The inventive structure is based on strained Si/SiGe interface that has high temperature super-conductivity. The first layer includes SiGe, such as $Si_{1-x}Ge_x$, where x is in the range of approximately 0.6 to approximat ly 0.8. The second layer also includes SiGe, such as $Si_{1-x}Ge_x$, where x is in the range of about 0.3 to about 0.4. The third layer includes Si. Illustratively, the first layer is under compressive strain, and the third layer is under tensile strain.

The layers are fully compatible with conventional structures for Si/SiGe CMOS. Thus, CMOS structures may be combined with the inventive structure, which acts as superconducting interconnects. In the inventive structure, adjacent layers of Si and SiGe are grown, such that electrons exist in the Si layer, and holes exist in the SiGe layers without recombining. Current is fed through the third layer, which is a Si channel, with electrons in it, and returned in an opposite direction through the first layer, which is a SiGe channel containing holes. Electrons and holes can be introduced by doping, modulation-doping, optically or using a field-effect from a top and/or bottom gate. This allows electrons and holes to move in the same direction, and due to the coulomb attraction, drag each other to form a superfluid. The inventive structure also includes electrical connections.

The present invention achieves high temperature superconductivity due to electron and hole pairing in the same structure without recombining. Superconductivity in the inventive structure results from electron-hole drag in the strained Si/SiGe layered structure. It is believed that conductivity of the inventive structure is sufficiently enhanced to produce superconductivity at temperature higher than would otherwise be possible in semiconductor materials.

Superconductivity is induced when equal densities of electrons and holes exist in adjacent channels. when the ratio of electron to hole densities is changed from equality, superconductivity is destroyed.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which:

FIG 1 shows a cross-section of a high temperature superconductivity structure having adjacent electron and hole channels according to the present invention;

FIG 2 shows a test structure for flowing current and measuring longitudinal and transverse magneto-resistance according to the present invention;

FIG 3 is a graph showing a nearly instantaneous large increase in current when the superconductor structure of FIG 1 turns on according to the present invention; and

FIG 4 is a graph showing nearly instantaneous large

increases in currents when the superconductor structure of FIG 1 turns on as a function of top and bottom gate biases according to the present invention.

FIG 1 shows a cross-section of a high temperature superconducting structure 10, according to one embodiment of the present invention. The structure 10 carries superconducting currents and includes a substrate 12. Illustratively, the substrate 12 is silicon (Si), which is doped p-.

A layer of silicon Germanium (SiGe) 14 is formed over the substrate 12. This $Si_{1-y}Ge_y$ layer 14 is graded, where y=0 at the interface 16 between the substrate 12 and the graded layer 14. At an opposite interface 18, i. e., opposite from the substrate-to-graded layer interface 16, the value of y is 0.3, for example.

A relaxed SiGe layer 20, such as an $Si_{0.7}Ge_{0.3}$ layer is formed over the graded layer 14. The relaxed layer 20 acts as a buffer layer. Illustratively, the graded and relaxed layers 14, 20 are each approximately 1000 nm thick.

A high temperature superconducting channel 22 is formed over the relaxed buffer layer 20. The superconducting channel 22 includes three epitaxial layers, namely, two semiconductor layers doped with different type dopants, separated by a barrier layer. Illustratively, a silicon channel 24 is formed over the buffer layer 20 having a thickness of approximately 10 nm. The silicon channel 24 is used to transport electrons 25. A pair of contacts 26, 28, which are silicon doped with N-type material for example, are formed at both edges of the silicon channel 24. The silicon channel 24 is under a tensile strain because the underlying substrate is a relaxed SiGe buffer. This is advantageous because the silicon under tensile strain of the Si channel 24 forms an electron quantum well, which confines the electrons.

A thin barrier layer 30 is formed over the silicon channel 24. The barrier layer includes $Si_{1-x}Ge_x$, where x is in the range from about 0.3 to about 0.4.

Next, an Si_{1-x}Gex layer 32 is formed over the barrier layer 30, and is used to transports holes 33. Illustratively, the P-type channel 32 has a thickness of approximately 10 nm, and x is in the range from about 0.6 to about 0.8. The SiGe P-type channel 32 is under a compressive strain because the underlying substrate is a relaxed SiGe buffer layer 20 with lower Ge-content. This is advantageous because the high Ge-channel 32 forms a hole quantum well, which confines the holes. The Si and SiGe channels 24, 32 are referred to as type II (staggered) aligned layers.

The P and N type channels 32, 24 may be inverted, where the P-type channel 32 is formed over the relaxed SiGe buffer layer 20, and the N-type channel 24 is formed over the thin barrier layer 30.

The barrier layer 30 is thick enough to restrict recombination of electrons 25 and holes 33 flowing in the N and P channels 24, 32, respectively, yet thin enough to allow coulomb force attraction between these electrons 25 and holes 32 to form electron-hole pairs. Illustratively the thickness of the barrier layer is from approximately 5 Å to approximately 30 Å.

A pair of P-type regions 34, 36, acting as P-type electrodes or contacts, is formed at the edges of the P-type channel 32. A top silicon layer 38 is formed over the P-type channel 32.

A DC bias in applied to the P and N contacts 34, 26 on one side of the channel 22, for example, using a battery 40. The P and N contacts 36, 28 located opposite the biased contacts 34, 26 are shorted together by a wire 42. These connections cause current to flow through the channel 22 as discussed in connection with FIG 2.

In accordance with the present inventions, the electron-hole pairing in the inventive structure 10, which is implemented with the Si/SiGe channels 24, 32, results in superconductivity. Superconductivity is induced when equal densities of electrons 25 and holes 33 exist in the adjacent channels 24, 32. when the ratio of electron to hole densities is changed from equality, superconductivity is destroyed. The inventive structure 10 achieves superconductivity in single crystal material that is fully compatible with semiconductor manufacturing and, in particular, with a recently suggested Si/SiGe CMOS process discussed in the following reference, which is incorporated herein by reference:

(1) U.S. patent number 5,534,713, issued on July 9, 1996, to Khalid Ismail and Frank Stern,entitled "CMOS Transistor Logic Strained Si/Ge Heterostructure Layers", and assigned to the same assignee hereof. The idea of electron-hole pairing, and the possibility of forming a superfluid has been generally suggested in the following reference, which is incorporated herein by reference:

(2) Yu.E. Lozovik and V.I. Yudson, "A New Mechanism for Superconductivity: Pairing Between Spatially Separated Electrons and Holes", Sov. Phys. JETP, vol 44, No. 2, pp. 389-397 (1976).

The essential requirements for forming such a superfluid is the following: (1) that the electrons and holes have similar masses and concentrations; (2) that they can co-exist without recombining; (3) that they are close enough for the coulomb interaction between them to be significant; (4) and that they move in the same directions, so that the currents in the N and P channels 24, 32 flow in opposite directions.

The strained Si/SiGe channels 24, 32 of the superconducting structure 10 are grown in such a way that electrons 25 are confined in the Si layer 24, and holes 33 are confined in the SiGe layer 32. The strain causes the electron and hole masses in the plane perpendicular to the growth axis to be different from their masses perpendicular to the plane along the growth axis. In the structure for CMOS discussed in the Ismail reference

(1) cited above; the effective electron mass in the plane is 0.2 me, and perpendicular to the plane is 0.96 me, where me is the electron mass. For holes 33,the corresponding masses are 0.15 me and 0.5 me, respectively.

The inventive superconducting structure 10 has great advantages over conventional superconducting structures to implement the electron-hole pairing structure. First, the type-two (staggered) band alignment of Si and SiGe layers 24, 32 makes it possible to confine and spatially separate the electrons 25 and holes 33. Second, the high perpendicular masses of electrons and holes facilitates separation of wave functions of both particles (i.e., electrons 25, and holes 33) by the very thin barrier 30.

In conventional material systems, which exhibit type-two band alignment, such as InAs/GaSb, the electron mass is very small, and hence a thick barrier is required. It is very advantageous to have a thin barrier in order to increase the coulomb attraction between the electrons and holes to form pairs. In the Si/SiGe channels 24, 32, the in-plane masses and mobilities of both electrons 25 and holes 33 are quite similar, which helps in forming a superfluid state. The inventive structure 10 is grown on Si substrates and is compatible with the recently suggested CMOS process discussed in the Ismail reference (1), and with conventional semiconductor manufacturing.

As shown in FIG 2, in order to form electron-hole pairs, the electrons 25 and holes 33 have to be moving in the same direction shown by arrow 48. Two currents flow in opposite directions as shown by arrows 46, 48.

Fig 2 is a test pattern or structure 50 for examining electron-hole drag, where current 52 flows into the N-type contact 26, through the channel 22 in direction 46 toward the N-type contact 28, to the P-type contact 36 through the wire 42, back through the channel 22 in direction 48 toward the P-type contact 34, and out of the P-type contact 34. The current flows in direction 46 in the lower part of the channel 22, corresponding to the N-type channel 24 of FIG 1, because the electrons 25 flow in a direction which is opposite to the current direction 46. Similarly, the current flows in direction 48 in the upper part of the channel 22, corresponding to the P-type channel 32 of FIG 1, because the holes 33 flow in the same direction as the current direction 48.

The test structure 50 is used for flowing currents and measuring longitudinal and transverse magneto-resistance of the electron and hole channels. The electrons and holes are forced to flow in the same direction, e.g., from contacts 28, 36 to contacts 26, 34. The test structure 50 is used as follows. A positive voltage is applied to the N-contact 26, contacts 28 and 36 are shorted together by the wire 42, and the P-contact 34 is grounded.

The occupation of the channels 24, 32 with electrons 25 and holes 33 can be induced by shining light on the sample, on the top silicon layer 38, with a wavelength that is in the range of approximately 1.0 μm to approximately 1.5 μm. This wavelength corresponds to the bandgap of the strained alloy SiGe in layer 32. The carrier density can also be controlled using a top gate 43 or a bottom gate 44 bias. Thus, the inventive device 10 can also be operated as a transistor in a three/four terminal configuration. In the three terminal configuration, P and N contacts 36, 28 are shorted together, while in the four terminal configuration, the four terminals are the four contacts 26, 34, 28, 36. The inventive device can be switched from a low conductivity state to a superconducting state while the supply bias 40 can be very low.

The inventive device can be used as an interconnect in circuits and in building Josephson junction devices and circuits, and in magnetic detectors. It can be also used as a very efficient photo-detector in the infrared, and for low power field-effect transistors.

In addition, the inventive device 10 can be used as a frequency multiplier or in multilevel logic, based on the non-monotonic increase in current with the gate voltage. FIG 3 shows the nearly instantaneous large increase in current 60 when the inventive superconductor device 10 turns on. This is in contrast to the monotonic current increase 62 for a typical conductor.

Further, the inventive superconductor device can be used as a comparator between the voltages on the bottom and top gates 44, 43. Superconductivity, and hence high current, are achieved only at a specific combinations of gate voltages. This is shown in FIG 4, where large currents 70, indicating superconductivity, occur at particular values of top and bottom gate voltages, Vg1 and Vg2, respectively.

The invention can be implemented by growing Si/SiGe heterostructure layers 24, 32, where the electrons 25 exist in a Si-layer 24 under tensile strain, and the holes are in the SiGe layer 32 under compressive strain. These layers are separated by the thin SiGe barrier layer 30 (about 1 nm thick) with Ge content of approximately half that of the P channel 34. That is,the value of x in the $Si_{1-x}Ge_x$ material of the barrier layer 30 is approximately half the value of x in the $Si_{1-x}Ge_x$ material of the P channel 34. Currents flow in opposite directions in those channels 24, 32 by passing successively through the external contacts 26, 28, 36, 34, for example.

Claims

1. A structure for carrying superconducting current comprising: a substrate;

   a first epitaxial P type semiconductor layer for transporting holes;

   a second epitaxial barrier layer positioned on said first layer, said barrier layer restricting the recombination of electrons while permitting coulomb forc attraction between lectrons

and said holes to form electron-hole pairs; and

a third epitaxial N type semiconductor layer for transporting said electrons.

2. The structure of claim 1, wherein said first layer includes SiGe and wherein said first layer is under compressive strain.

3. The structure of claim 1, wherein said second layer includes SiGe having a thickness in the range from about 5 to 30 Angstroms.

4. The structure of claim 1, wherein said third layer includes Si and wherein said third layer is under tensile strain.

5. The structure of claim 1, wherein said first layer includes $Si_{1-x}Ge_x$, where x is in the range from about 0.6 to about 0.8.

6. The structure of claim 1, wherein said second layer includes $Si_{1-x}Ge_x$, where x is in the range from about 0.3 to about 0.4.

7. The structure of claim 1, wherein said substrate includes a graded layer and a buffer layer formed between said graded layer and said third layer.

8. The structure of claim 7, wherein said graded layer includes $Si_{1-y}Ge_y$, where y is in the range from about 0 to about 0.3.

9. The structure of claim 7, wherein said buffer layer includes $Si_{0.7}Ge_{0.3}$.

10. The structure of claim 1 further including a fourth epitaxial barrier layer, and wherein said first through fourth layers are repeated.

11. The structure of claim 1 further comprising a bottom gate located below said substrate, and a top gate located above said third epitaxial N type semiconductor layer.

12. The structure of claim 10 wherein voltages on said top and bottom gates induce superconductivity.

13. The structure of claim 10 further comprising a top silicon layer formed between said top gate and said third epitaxial N type semiconductor layer.

14. The structure of claim 1 further comprising a light source for shining a light of predetermined wavelength to induce superconductivity.

15. The structure of claim 13, wherein said predetermined wavelength is in the range of approximately 1.0 μm to approximately 1.5 μm.

16. A field effect transistor for carrying superconducting current comprising the structure of claim 1.

17. The field effect transistor of claim 16 further including a gate electrode positioned adjacent one of said first and third layers and wherein said first and third layers are coupled together on one side of said gate electrode.

18. A comparator having a structure for carrying superconducting current as claimed in claims 1 to 15.

19. A magnetic detector having a structure for carrying superconducting current as claimed in claims 1 to 15.

20. A photo-detector having a structure for carrying superconducting current as claimed in claims 1 to 15.

21. The photo-detector of claim 20 further including a radiant energy source and a light path for directing radiant energy from said radiant energy source to said first and third layers.

22. A frequency multiplier having a structure for carrying superconducting current as claimed in claims 1 to 15.

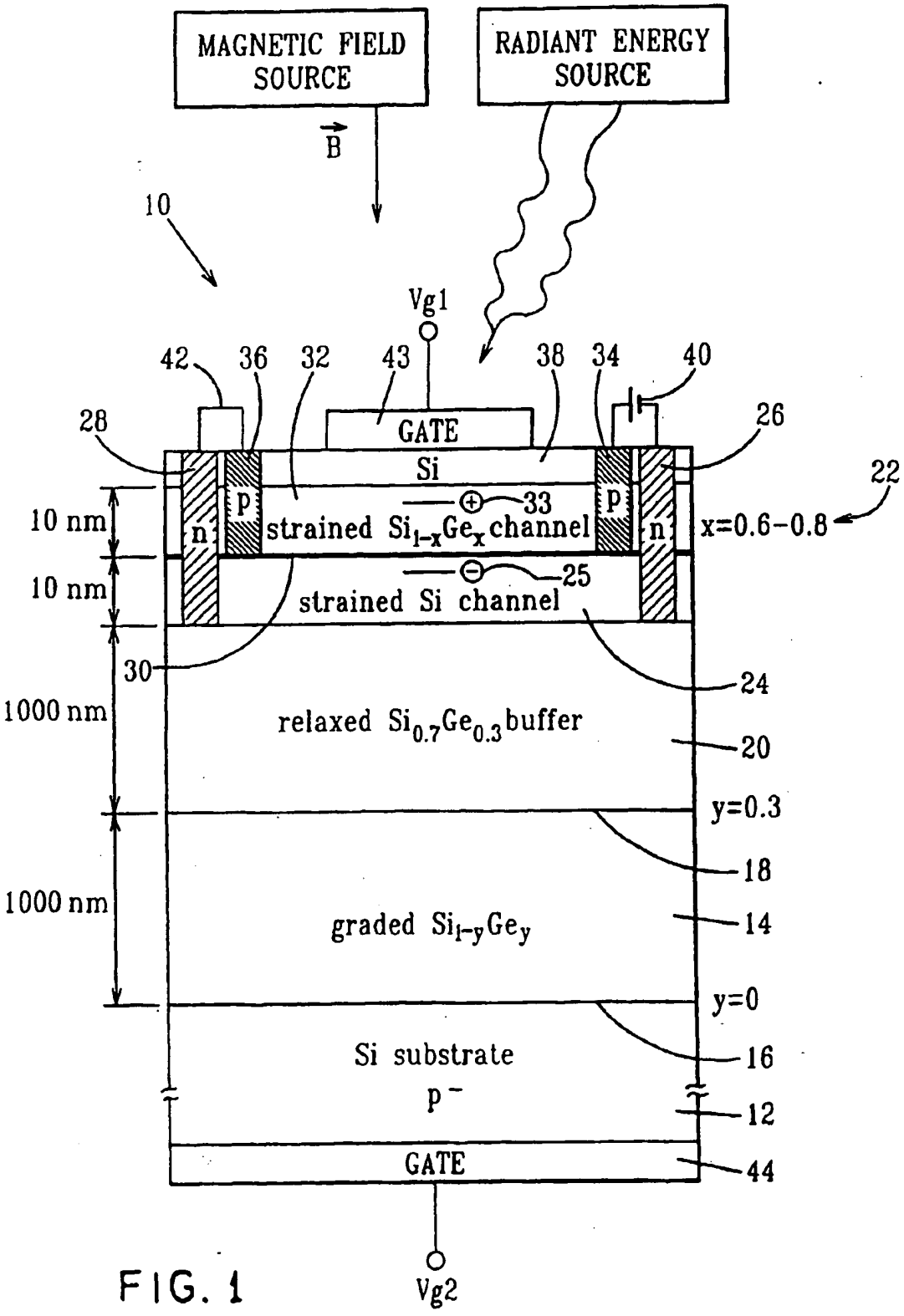
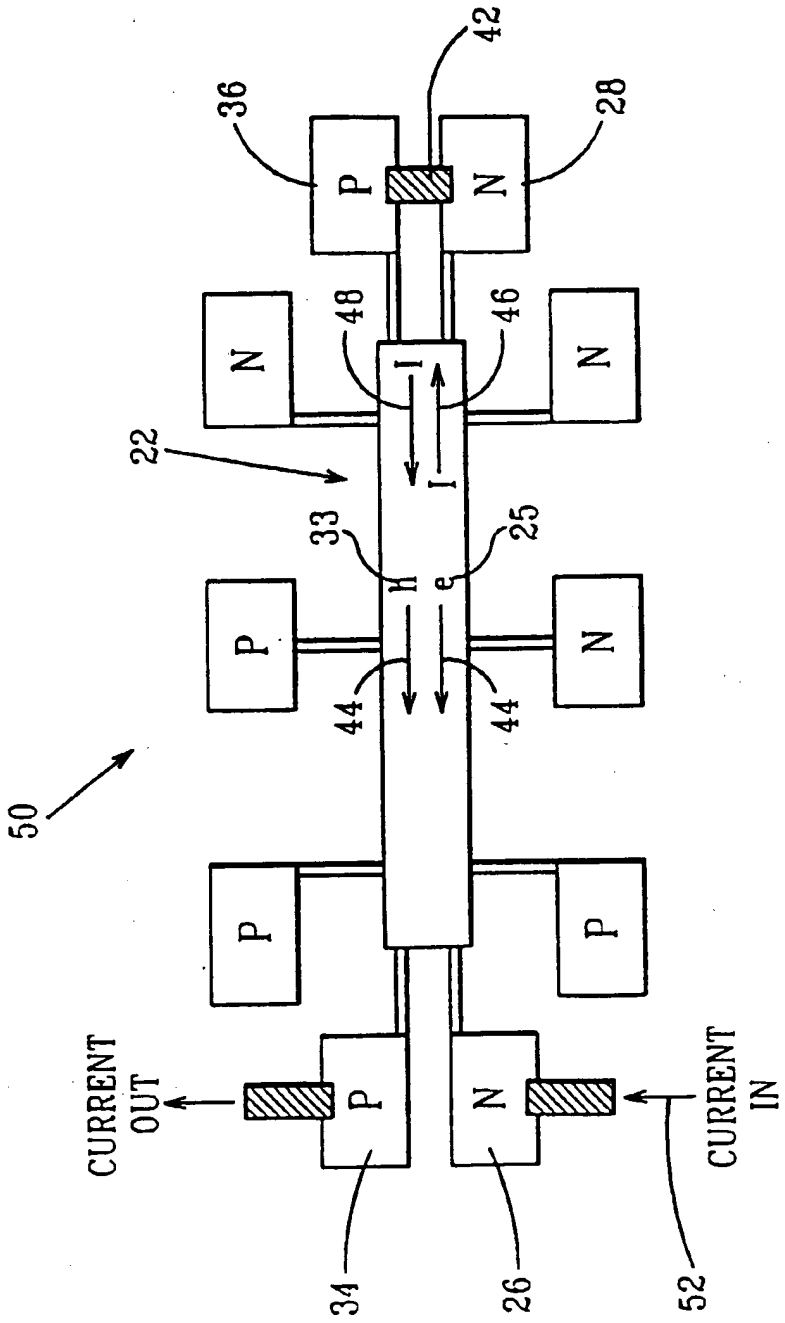

MAGNETIC FIELD SOURCE
RADIANT ENERGY SOURCE
B
10
Vg1
42
36
32
43
38
34
40
28
GATE
26
Si
22
10 nm
p
33
p
n
strained $Si_{1-x}Ge_x$ channel
n
x=0.6-0.8
10 nm
25
strained Si channel
30
24
1000 nm
relaxed $Si_{0.7}Ge_{0.3}$ buffer
20
y=0.3
18
1000 nm
graded $Si_{1-y}Ge_y$
14
y=0
Si substrate
p^-
16
12
GATE
44
Vg2

FIG. 1


42
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50
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CURRENT OUT
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CURRENT IN
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FIG.2

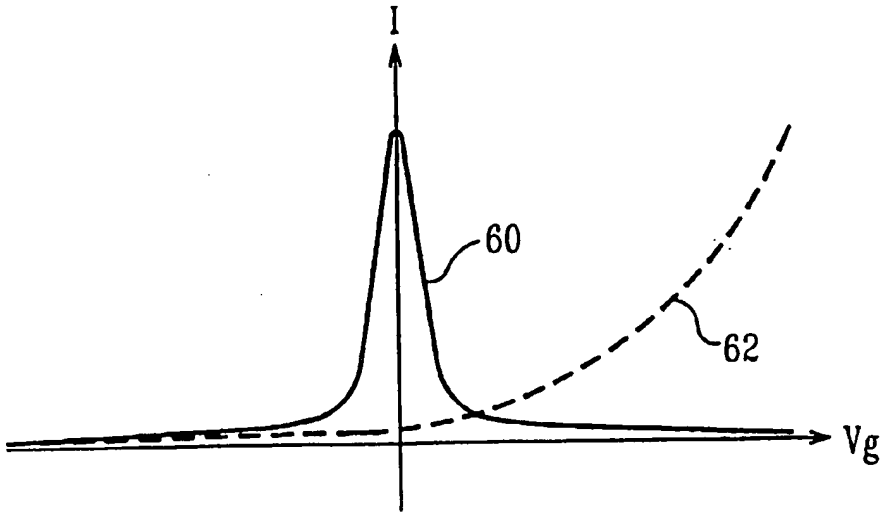

FIG. 3

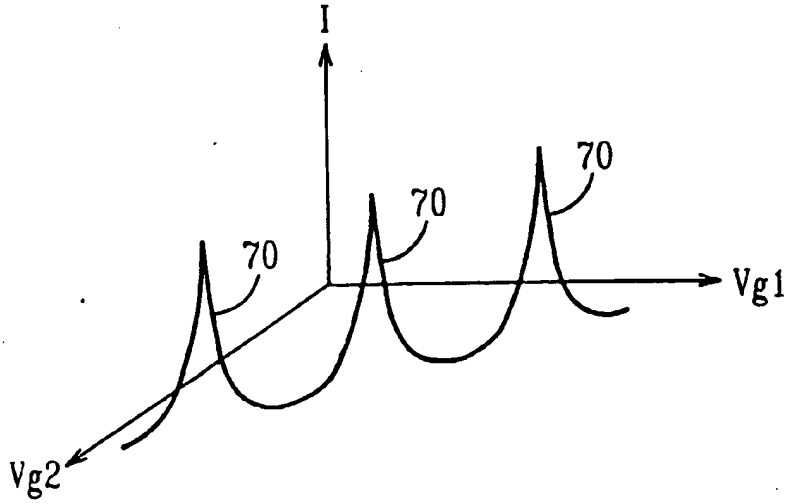

FIG. 4